	US ATLAS **PHASE II Upgrade** **BASIS of ESTIMATE (BoE)**	**Date of Est: 10/22/2015** **Rev 10/22/2015** **Prepared by: J.Ye** **Responsible Inst: SMU** **Docdb #:**

WBS number: **LArFE_SMU**	**WBS Title:** LArFE_SMU, SER, OTx Data Link and Control Link

WBS Dictionary Definition: Develop the data link and adapt the control (TTC) link from LTDB for the FEB in the phase-2 upgrade. Other than the design and testing of the two link systems, there will be ASIC development of the serializer and the optical transmitter OTx which consists of a VCSEL driver and VCSEL array together with the optical coupling components.

Estimate Type (check all that apply – see BOE Report for estimate type by activity):

___ Work Complete
_x_ Existing Purchase Order
_x_ Catalog Listing or Industrial Construction Database
_x_ Documented Vendor Estimate based on Drawings/ Sketches/ Specifications
_x_ Engineering Estimate based on Similar Items or Procedures
_x_ Engineering Estimate based on Analysis
_x_ Expert Opinion

Supporting Documents (including but not limited to):

Assumptions and component counts:

One FEB reads out 128 LAr detector channels. Assume each channel is read out with two14-bit 80 MSPS ADCs, one for the high gain and the other for the low gain. This leads to a raw data rate of 2.24 Gbps. Assume 30% bandwidth overhead for serial data transmission framing, forward error detection code, and event building (including BCID info), this give a total bandwidth requirement of each FEB to be 372.736 Gbps. In this WBS, SMU is responsible for the development of the serializer ASIC, the optical transmitter module OTx, and design of the data link, and the adaptation of the Control Link (TTC link) from LTDB. We further assume that the serializer will operate at 10 Gbps per channel, and 2 channels will be packaged in a single QFN (likely QFN-100) package; the OTx will be array optics based and each has 10 fiber channels. Under these assumptions there will be 20 serializer chips and 4 OTx modules for each FEB. Follow the current ATLAS policy of 8% spare boards and 8% spare components, we will need 35,357 serializer chips and 7,072 OTx modules for the whole LAr detector front-end readout data links. We assume that there will be one control link for each FEB.

We assume that all the wafer production will be coordinated at the level-2 level, if not at US-ATLAS level, so we only take into account the packaging cost of the serializer and the assembly cost of OTx. We do not count in the wafer production.

Details of the Base Estimate (explanation of the work)

We rely on the IP blocks developed for lpGBT for the LAr FEB dedicate serializer ASIC development. This serializer ASIC will contain a dedicated interface to the ADC chosen by LAr for FEB. It will also contain a GBT-like framing and FEC so that we can take advantage of the GBT standard FPGA code for the back-end. We plan to place two serializing units in one die, sharing one PLL, as we do in the LOCx2 serializer for LTDB, to save on power and packaging cost. The design of OTx benefit from the developments of the ATx in the CDRD project with FNAL, and the R&D in the Versatile Link+ common project. OTx will use a 10-lane VCSEL array with a matching driver ASIC. Both the serializer ASIC and the driver ASIC will be developed using the TSMC 65 nm CMOS technology, identified by CERN.

ASIC designer will be needed for the ASIC work. As we rely on work already carried out in lpGBT, CDRD and the VL+ projects, we anticipate only 1 designer FTE for the first 3 years and that reduces to 0.5 FTE for the last 2 years. A Sr. engineer and a Jr. engineer will be needed for testing the ASIC prototypes, OTx modules, their productions and QAs, and for design evaluations of the two link systems. We anticipate the need of 0.5 FTE of the Sr. engineer for the first 3 years. That increases to 1 FTE in the 4^{th} year mostly for production related work. The 5^{th} year, we anticipate only 0.5 FTE of the Sr. engineer to transfer knowledge during installation to M&O. We anticipate 1 FTE for the first 4 years to carry out test related tasks (PCB designs, conducting tests, including necessary irradiation tests). During the production QA, due to the huge number of chips and OTx modules that will need to be tested, we anticipate the need of 2 student FTEs for the period from the 2^{nd} year to the 4^{th} year.

M&S covers material cost in ASIC prototyping, test chip packaging, PCBs and their assembly (including component costs), materials in lab and irradiation tests (this includes shared proton beamtime). The QFN packaging cost of the serializer is taken from the quote for LOCx2, also a QFN-100 packaging. OTx cost is based on the parts and wire-bonding service. The cost for the control link is based on the cost of the similar link for LTDB.

The core cost is estimated assuming 100% packaging efficiency:

Packaging of the serializer

NRE	$1,500	
Tooling	$4,000	
QFN frame	$1	$2000 for every 3000 frames
Tray	$0	$200 for a trays of 3000 chip
Packaging lot	$5	$1000 for 200 chips in a lot
Total 35,357 chips	$208,900	

OTx parts and wire bond service

MOI	$7
Prizm	$48
VCSEL (12-lanes)	$104
PCB	$5
ZA8 (connector and accessaries)	$13
Assembly (wire bond)	$40
Cost of each OTx	$217
total 7072 OTx	$1,533,705

Control Link

GBTx	$55
GBT-SCA	$26
VTRx	$220
cost of one link	$301
total of 1524 control links	$459,334

total core cost	$2,201,938